

In The Claims:

1. (original) A non-volatile memory, comprising:
a substrate;
a word-line on the substrate;
a charge trapping layer between the substrate and the word-line;
a contact disposed over the substrate electrically connecting with the word-line; and
a protective metal line electrically connecting with the contact and with a grounding doped region in the substrate, wherein the protective metal line has a first resistance higher than a second resistance of the word-line.
2. (original) The non-volatile memory of claim 1, wherein the protective metal line has a first width smaller than a second width of the word-line.
3. (original) The non-volatile memory of claim 1, wherein the protective metal line has a first thickness smaller than a second thickness of the word-line.
4. (original) The non-volatile memory of claim 1, wherein the protective metal line is electrically connected with the grounding doped region via another contact.
5. (original) The non-volatile memory of claim 1, wherein the charge trapping layer comprises a silicon oxide/silicon nitride/silicon oxide (ONO) composite layer.
6. (original) The non-volatile memory of claim 1, wherein the word-line comprises:
a polysilicon line on the charge trapping layer; and
a metal silicide line on the polysilicon line.

PATENT

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7. (original) The non-volatile memory of claim 6, wherein the metal silicide line comprises tungsten silicide (Wsi_x).

Claims 8-14 (canceled)